

TECHNICAL REPORT



Device embedding assembly technology
Part 2-7: Guidelines – Accelerated stress testing of passive embedded circuit boards

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TECHNICAL REPORT



Device embedding assembly technology
Part 2-7: Guidelines – Accelerated stress testing of passive embedded circuit boards

INTERNATIONAL
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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY

**Part 2-7: Guidelines – Accelerated stress testing of
passive embedded circuit boards**

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IEC TR 62878-2-7, which is a technical report, has been prepared by IEC technical committee 91: Electronics assembly technology.

The text of this technical report is based on the following documents:

Enquiry draft	Report on voting
91/1553/DTR	91/1559/RVDTR

Full information on the voting for the approval of this technical report can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all parts in the IEC 62878 series, published under the general title *Device embedding assembly technology*, can be found on the IEC website.

Future standards in this series will carry the new general title as cited above. Titles of existing standards in this series will be updated at the time of the next edition.

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DEVICE EMBEDDING ASSEMBLY TECHNOLOGY

Part 2-7: Guidelines – Accelerated stress testing of passive embedded circuit boards

1 Scope

This part of IEC 62878 describes the accelerated stress testing of passive embedded circuit boards. It can be used for screening finished boards, including multilayer and high-density interconnection (HDI) boards. These boards are mainly for mobile devices.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60194, *Printed board design, manufacture and assembly - Terms and definitions*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in IEC 60194 apply.

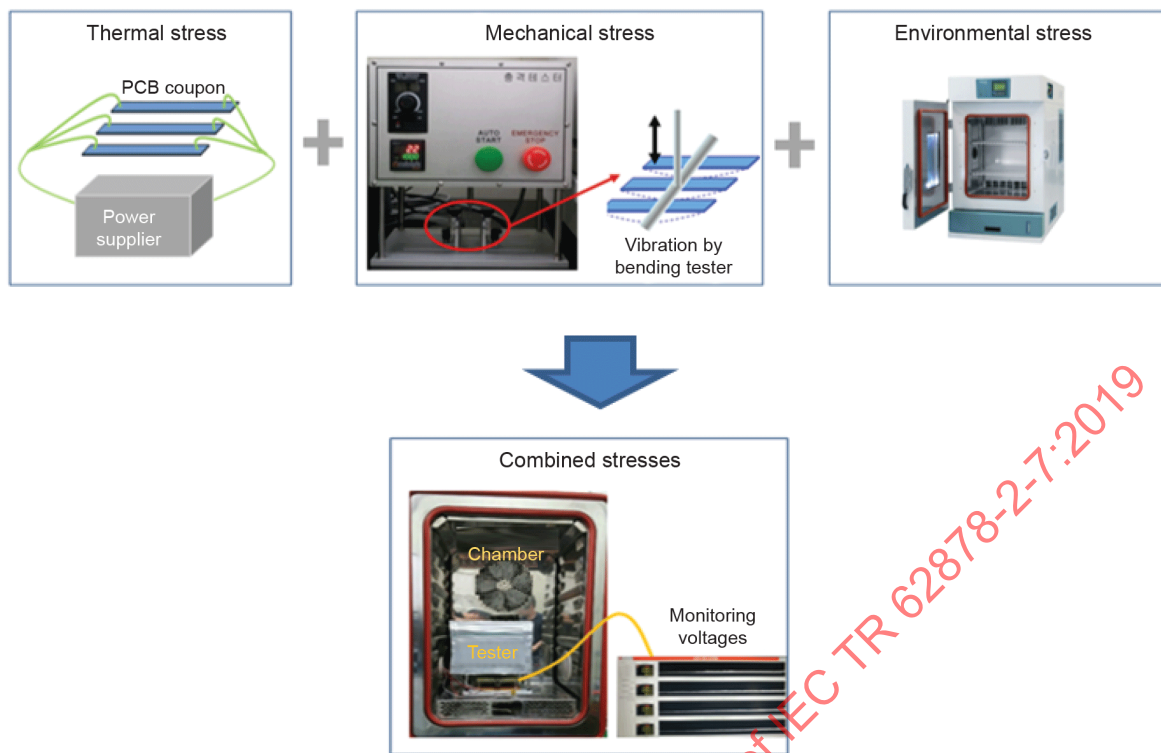
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- IEC Electropedia: available at <http://www.electropedia.org/>
- ISO Online browsing platform: available at <http://www.iso.org/obp>

4 Overview of accelerated stress testing of passive embedded circuit boards

4.1 Testing under combined stresses

A combined test method has been used to simulate real world conditions. It is a combination of a thermal stress by heating at high temperature, an environmental stress at 85 °C/ 85 % RH, and a mechanical stress with vibration. In order to test specimens under various stresses, a bending tester with heat generating specimens was put into the thermo-hydrostat. The reliability can be checked by monitoring output voltage of the heated sample as shown in Figure 1. The heating temperature is set to 325 °C in order to shorten the testing time to 1 h for boards fabricated with a high temperature of decomposition (T_d) material ($T_d > 350$ °C). The testing can be done at 305 °C for 1,5 h if material with a lower T_d is used.



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Figure 1 – Testing principal

4.2 Test coupon design

Four test coupons are built in a test area of passive embedded circuit board panel as shown in Figure 2. Each test coupon has circuits connecting embedded passives, as shown in Figure 3, that act as heating circuits as well. They are fabricated in accordance with the design rules in Annex A. The design and layer specifications are shown in Tables 1 and 2. The circuits of the top and the bottom layers are the same.



- ✖ Test panel information
- Size: 610 mm × 450 mm
 - Number of layer: 4 L

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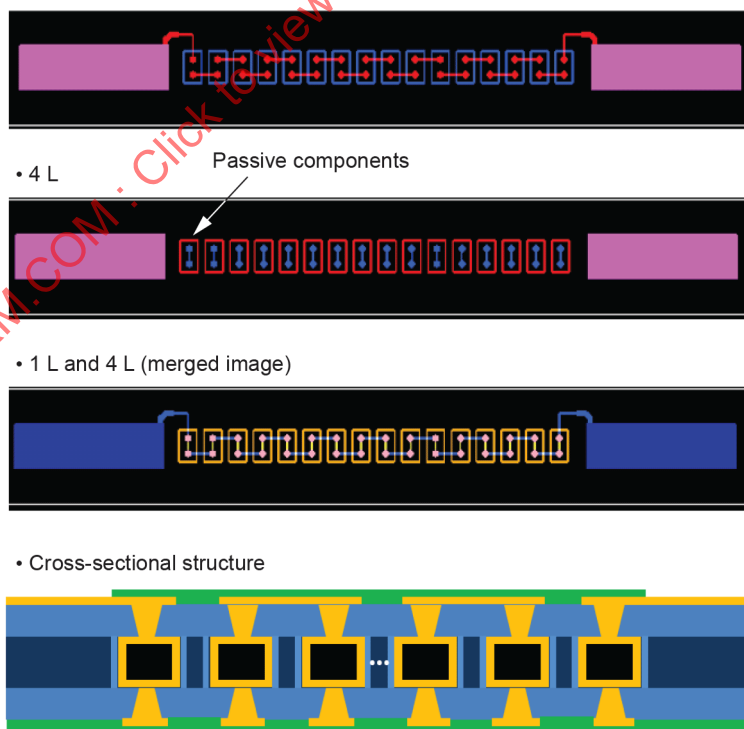
Figure 2 – Embedded circuit board panel with test coupons

Table 1 – Design information for test coupon

Line width	100 µm
Via pad	350 µm
Distance between embedded components	450
Ground connection size	7,28 mm × 2 mm
Coupon size	35 mm × 5 mm

Table 2 – Stack-up information for test coupon

Layer	Thickness (µm)
Solder resistor	20
Circuits (copper)	30
Dielectric (prepreg)	60
Circuits (copper)	35
Dielectric (FR4 core)	250
Circuits (copper)	35
Dielectric (prepreg)	60
Circuits (copper)	30
Solder resistor	20
Total	540 ± 54



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Figure 3 – Test coupon structure

5 Test procedure

5.1 General

For testing, the power supply was connected to the ground contact part of the coupon through wire. The output was monitored using a data gathering module and displayed on the monitor in real time. Dynamic bending testing was carried out using the test equipment in Annex B.

5.2 Setting test temperature

The temperature of the test coupon was controlled by changing the electric current. The target temperature was set by applying a predetermined current to the coupon. The test setting was 325 °C for 1 h.

- a) The temperature of the test coupon was controlled by a changing electric current.
- b) The target temperature was set by applying a predetermined current to the coupon.
- c) To check the temperature, the thickness side of coupon was grinded until vias were exposed.
- d) Coupons were heated by applying the current.
- e) The temperature of the coupon was measured by an IR thermometer.
- f) The input current can be obtained by monitoring the temperature with varying current.
- g) In the case of the described coupon, the desired 325 °C corresponded to 1,2 A.

5.3 Placement of samples on bending tester

The coupons were placed in a sample jig as shown in Figure 4. The bending tester was in validated calibration condition, and is capable of vibration and bending.

- a) The cover of the sample jig was opened.
- b) The cover was closed after four coupons were inserted into the slots on the jig
- c) The jig with coupons was placed in the bending tester.
- d) The jig was fixed to the bending tester by tightening screws at corners.
- e) The height of bending jig is adjusted so that the tip of the jig is in contact with coupons.



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Figure 4 – Opened and closed sample jig

5.4 Imposing combined stresses

The bending tester with specimens was placed in a temperature humidity chamber as shown in Figure 5. The environment chambers were in validated calibration condition, and using DI water for the chamber. 2-mm bending is used for a typical MLCC. 1-mm bending can be used for MLCC thinner than 150 µm.

- a) The sample jig was connected to a power supply and a voltage tester.
- b) The temperature was set to 85 °C and humidity at 85 % RH; the chamber was allowed to stabilize.
- c) The bending tester was set to 2-mm bending with 15 r/min and turned on.
- d) A constant current of 1,2 A was applied at one terminal and the voltage was monitored at the other terminal.
- e) The temperature of the circuits inside reached 325 °C within a minute while the surface temperature was much lower (~210 °C).
- f) The test was terminated after 1 h by turning off the power supply, bending tester and the chamber.

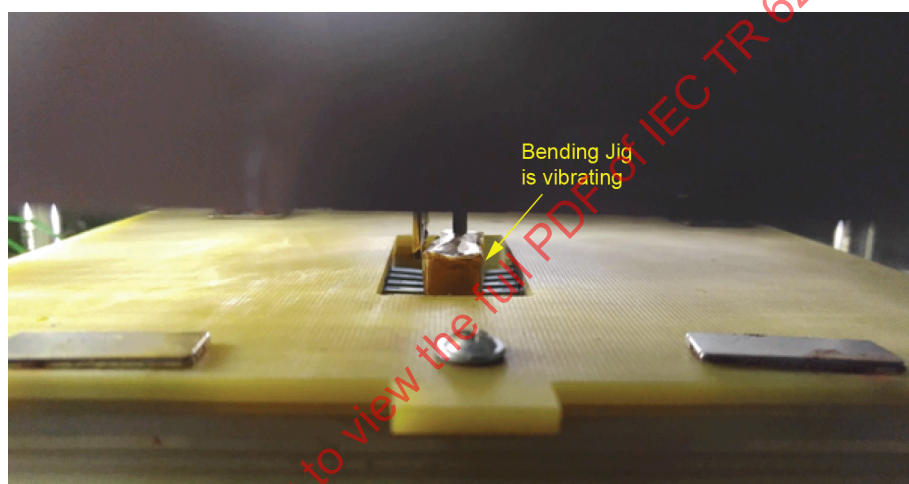


Figure 5 – Bending of test coupons

5.5 Evaluation of results

There is resistance increase due to the failure. And the voltage was monitored to check the resistance change. The criterion for failure is an increase of more than 20 % of the output voltage.

- a) The voltage signal graphs of each coupon were checked for the stability of the output. If the change is less than 20 %, then the sample is passed. If the change is more than 20 %, then the sample is no good, as shown in Figure 6.
- b) All failed specimens were evaluated by cross-sectioning the via area.
- c) All test results and cross section photos were recorded and stored.

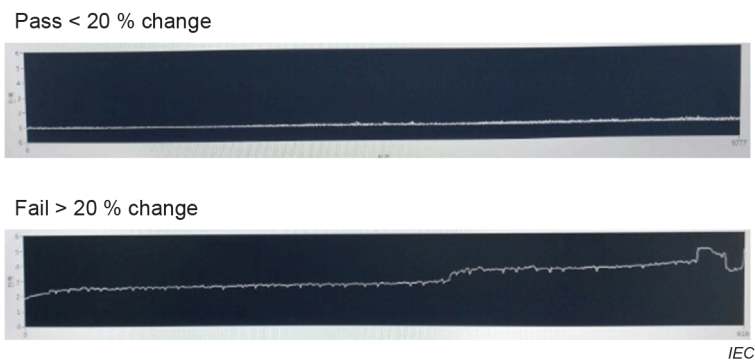


Figure 6 – Output voltage

6 Results

The results of testing 300 coupons are summarized and presented in Table 3 and Figures 7 and 8. There are neither voids nor delamination due to thermal degradation after testing, as shown in Figure 7. The failed coupons had via cracks.

Table 3 – Coupon testing results

Sample lot #	Sample Size	Result	Remark
Lot #1	100 pcs	All pass (100/100 pcs)	
Lot #2	100 pcs	All pass (100/100 pcs)	
Lot #3	100 pcs	Pass (96/100 pcs)	NG (4pcs)

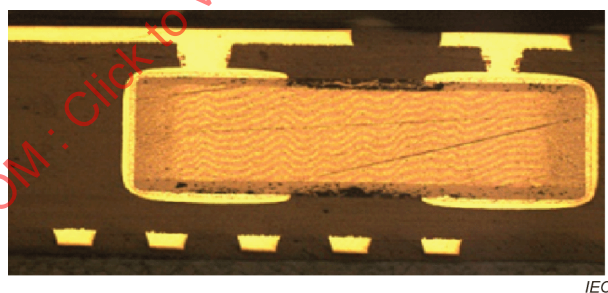


Figure 7 – Cross section of sample after testing

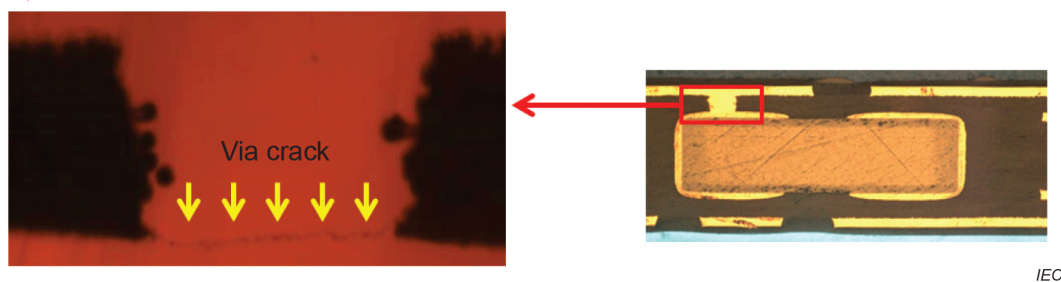


Figure 8 – Cross section of failed sample