SAE The Engineering Society For Advancing Mobility Land Sea Air and Space®
INTERNATIONAL
400 Commonwealth Drive, Warrendale, PA 15096-0001

SURFACE VEHICLE INFORMATION REPORT

SAE J2628

ISSUED AUG2002

Issued 2002-08

Conducted Immunity—Design Margins and Characterization

1. ***Scope—***This document establishes a method for characterizing the design margins and compatibility of electronic devices and equipment used in vehicles to various voltage fluctuations and transients over temperature.

2. ***References***

2.1 **Applicable Publication—**The following publication forms a part of this specification to the extent specified herein. Unless otherwise indicated, the latest issue of publications shall apply.

2.1.1 SAE PUBLICATION—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J1113-1—Electromagnetic Compatibility Measurement Procedures and Limits for Vehicle Components (Except Aircraft)

2.2 **Related Publications—**The following publications are provided for information purposes only and are not a required part of this document.

2.2.1 SAE PUBLICATION—Available from SAE, 400 Commonwealth Drive, Warrendale, PA 15096-0001.

SAE J1113-11—Immunity to Conducted Transients on Power Leads

2.2.2 ISO PUBLICATION—Available from ANSI, 25 West 43rd Street, New York, NY 10036-8002.

ISO 7637-3—Road vehicles—Electrical disturbance by conduction and coupling

3. ***Definitions—***See SAE J1113/1

3.1 **LOL/UOL-X (Y)—**Lower and Upper Operating Limit (when DUT ceases to operate or is erratic) for parameter X at specified conditions Y. For example LOL-V (T-hi) = Lower Operating Limit for voltage at T-hi temperature.

TO PLACE A DOCUMENT ORDER:
Tel: 877-606-7323 (inside USA and Canada)
Tel: 724-776-4970 (outside USA)
Fax: 724-776-0790
Email: custsvc@sae.org
SAE WEB ADDRESS: http://www.sae.org

4. ***Measurement Philosophy—***The methods used are designed to address some of the deficiencies inherent in other commonly used methods. Specifically, EMC testing is most commonly run at room temperature due to the nature of the test equipment and facilities. This is a major concern for conducted immunity testing where the response of the product could be different when cold or hot than at room temperature.

Another characteristic of typical EMC testing is that very repeatable, accurate and idealized signals are used to represent the “real world”. While this would appear to be desirable, it is not necessarily the case. The “real world” contains randomness and other characteristics (e.g., complex impedances) not replicated by such idealized test signals. This randomness is extremely critical for a microprocessor type DUT since the stress event (e.g., transients) must often line up in time with a certain point(s) in software execution to have an effect.

To address these deficiencies an alternate approach is specified that uses relatively simple and low cost techniques that does not require a laboratory environment. This makes it easier to identify concerns early during the development stage (although they can be used at any stage).

It is important to note that many of these tests are not the “test for success” type where the results are classified as either pass or fail. Such testing is of limited value since it generates little information. The goal here is to generate as many anomalies as possible so that the maximum amount of information is obtained.

5. ***Test Equipment***

5.1 **Electrical Stress Simulator—**See Figures 1 and 2.

a. Chattering Relay(s)—A key enabler for the methods used in this document is the “chattering relay” (Normally Closed relay contacts connected in series with the relay coil). It has the following characteristics:

1. Creates randomness.
2. Creates the actual complex mechanisms of the real event (e.g., contact arcing)
3. Simple, low in cost
4. Makes it practical to be used in multi temperature testing.

Characteristics:

1. Coil is 12 V AC (contains shading pole) operated at 12 V DC
2. R = 20 Ω nominal, Inductance = 100 to 150 mH at 60 Hz
3. Contact rating = 10 A (typical), DPDT

b. Ground, Power Resistors—Default = 10 W, 0.1 Ω, wirewound
c. High current inductive load used to create transients = A/C Clutch Coil

1. R-nom = 3 Ω
2. Inductance-nominal = 50 mH at 100 Hz.

d. DC Power Amplifier—DC - 20 kHz (3 dB), Range = 0 to 20 V nominal (for 12 V systems), current capability consistent with DUT. Can be constructed with power Op Amps (e.g., LM12CLK) and switching power supplies.
e. Waveform Generator—Able to create waveforms specified in this document.
f. Control Circuitry—Complexity depends on degree of automation (i.e., manual or computer control).
g. Although not mandatory, for ease of implementation, a single unit can be constructed to combine the essential components (items a to f previously) required for this testing - Product Assurance Robustness (PAR) tester. It contains three basic sub units:

Microprocessor (PC 104) controller with built in waveform generator.
Relays in a number of configurations one of which is a chattering relay.
DC Power Amplifier using switching power supplies and power op amp IC’s.

h. Variable DC Power Supply (test 6.4.1)—Capable of providing specified voltages at DUT current requirements. Shall not be affected by electrical noise simulator .
i. Data Acquisition—Capable of monitoring the DUT signals and tracking when the DUT response exceeds predetermined limits. Shall also log stress conditions when these limits are exceeded.
j. Thermal Chamber—Capable of temp range required and nominal ramp rate of 3 to 5 °C per minute.

6. Test Procedures

6.1 General Test Setup

a. Before a test plan is developed, the DUT shall undergo a Design Review by technical experts to determine where testing should be focused.
b. The test setup is shown in Figure 1. The DUT shall be connected to the actual operating devices (loads, sensors, etc.) using a test harness or the production wiring harness, as agreed upon between the vendor and the customer. If the original operating devices are not available, they may be simulated by methods outlined in SAE J1113-1. For tests involving a temperature chamber, the wiring harness from DUT to load fixture shall be long enough to place DUT in the thermal chamber.
c. For many of these methods, system and interface issues shall be addressed. Typical examples are:

1. Solenoid coil increase in resistance with temperature.
2. Wiring-connector resistance-inductance in ground and/or power circuits (default: 0.1 Ω, use a wirewound resistor to address inductance).
3. Switch series-parallel resistance (default: closed switch = 50 Ω, open switch = 50k Ω).

d. All voltages are measured at the DUT (PAR tester has resistance inserted in the power and ground circuits)
e. For many tests, the DUT must be operated in DUT mode(s) in awake, sleep or off state that is consistent with what the test represents (vehicle condition in accessory, off, start, run state).
f. Place DUT in typical operating mode (most temp, voltage sensitive) and monitor key output signals:

1. For DUT's with communications bus, connect communications bus analyzer and oscilloscope (look for magnitude changes). Operate DUT in mode that creates near maximum bus activity.
   NOTE— Communications Bus analyzers can be sensitive to electrical noise and may need filtering or optical coupler.
2. If the DUT exhibits abnormal behavior during testing, monitor appropriate internal DUT signals to determine root cause. Some examples are: Resets, low voltage inhibits, comparators, Vdd, EEPROM writes, load management enables-disables.

6.2 Test Equipment Tolerances—Characterization

Tolerances (unless otherwise specified):

Voltage = ±0.5 V, Time, Resistance = ±10%, Temperature = ±2 °C

A different approach is required for tests involving the chattering relays. Even though these tests are intentionally very random in nature (its real advantage) experience has shown that the DUT responses are very repeatable. The voltage waveforms produced should be periodically observed with an oscilloscope to verify correct waveform characteristics. The amount of degradation over time is a function of the currents that the relay contacts must provide to the DUT and how much the relay is used. Compare the characteristics when new and used with the following as a guide.

Chattering relay characteristics, refer to Figure 3:

a. Oscillation Frequency = 50 to 150 Hz
b. Duty Cycle = 30 to 70 %.

Transient characteristics using A/C coil specified in 5.1a with chattering relay (open circuit), refer to Figure 4:

a. Amplitude = –200 to –300 V maximum
b. Pulse width = 0.2 to 0.5 ms (between 10% points).

For the tests requiring use of the DC power amplifier, verify accuracy of the output waveforms both open circuit and loaded. The loaded waveforms should draw similar currents that the DUT would (default = 10 Ω). Maximum change from open circuit to loaded (amplitude, frequency response) = 10%.

6.3 Acceptance Criteria—The DUT shall, in general, be monitored continuously to a degree necessary to observe responses to stresses including diagnostic codes if applicable. This can range from simple visual observation to a Data Acquisition system including a communications bus analyzer. Performance Classifications defines the operation of the DUT during and after exposure to disturbances. By classifying the performance of a component in this manner, the acceptability is determined. Performance classifications are defined as follows (slightly modified from SAE J1113-1, Appendix A, differences are underlined):

a. Performance Class I: The function shall operate as designed during and after exposure to a disturbance.
b. Performance Class II: The function may deviate from design during exposure to a disturbance but will automatically return to normal after the disturbance is removed. Safe operation of the vehicle shall not be affected. No effect on permanent memory. Normally, no effect on temporary memory unless per design requirements.
c. Performance Class III: The function may deviate from designed performance during exposure to a disturbance but simple operator action may be required to return the function to normal once the disturbance is removed. Safe operation of the vehicle shall not be affected. No effect on permanent type memory is allowed.

Many of the tests are not a simple pass-fail type. Instead, they are discovery types of tests that are meant to produce the maximum amount of information (the more anomalies the better). This promotes a much better understanding of the DUT. The following are commonly used as acceptance criteria for this type of testing:

a. No LU = No Lock-up
b. No DTC = No false Diagnostic Trouble Codes (DTC)
c. Pre = Respond in predetermined manner.

6.4 Test Procedures

6.4.1 DESIGN MARGINS, CHARACTERIZATION—This method addresses the following:

a. Characterizes DUT operation over voltage and temperature ranges (design margins).
b. Verifies that the DUT is compatible with various types of electrical noise over DUT voltage and temperature ranges.

Special Equipment:

a. Thermal Chamber
b. Variable DC voltage source.
c. DUT Termination Fixture
d. Electrical Stress Simulator - PAR Tester

Evaluation Method:

T-ambient:

a. At T-ambient, apply ramp voltage from V-nom to 20 V and down ramp voltage to 0 V and back up to V-nom). Ramp rate = approx 10 V per minute. Ramp must be linear, not course digital steps. There are two test method options:

1. Manually using a variable power supply.
2. Use PAR tester. Connect CPU signal generator output (ramp) to DC power amplifier input. Connect DUT to DC power amplifier output.

b. Determine following values and verify predictable response throughout voltage ramp:

LOL-V (T-amb), (i.e., LOL – Voltage at T-amb)
UOL-V (T-amb), (i.e., UOL – Voltage at T-amb). Note if DUT still operational at 20 V.
NOTE— These limits are where DUT operation is erratic or ceases to operate.

c. Connect PAR Tester to power inputs of DUT, one at a time. Activate PAR Tester per evaluation method specified in 6.4.2.
NOTE— Ensure that Power Supply and DUT active terminations (e.g., signal generators) are not affected by noise generator.

d. Repeat steps a to c on a second DUT and verify similar results.

T-low:

e. Insert DUT into temperature chamber and lower temperature to DUT specified lower operating limit (at Vnom). Note operation during temp transition. Dwell at low temperature with power off until DUT temperature stabilizes (typically 10 minutes). Power up DUT at V-nom and verify proper start up and operation. Step to next lowest temperature (with DUT power off) and again verify proper start up and operation after temperature stabilization. Repeat stepping to determine LOL-T (V-nom).
NOTE— Keeping power off until temperature stabilized is important for achieving proper DUT internal temperatures and verifying start up characteristics. Step size = 5 °C from DUT specified lower operating limit. Limit lower temperature to 15 °C below specified DUT lower operating temperature.

f. Compute T-lo = LOL-T (V-nom) +5 °C. The value of T-lo should result in full module operation but not necessarily meet all specs.

g. Repeat Ramp and PAR testing at T-lo. Verify results are similar to that found in steps a to c.

LOL-V (T-lo), (i.e., LOL – Voltage at T-lo)
UOL-V (T-lo), (i.e., UOL – Voltage at T-lo). Note if DUT still operational at 20 V.

h. Repeat step g (at T-lo only) on second DUT and verify similar results.

T-high:

i. Increase temperature to DUT specified upper operating limit (at V-nom). Note operation during temp transition. Dwell at high temperature with power off until DUT temperature stabilizes (typically 10 minutes). Power up DUT at V-nom and verify proper start up and operation. Keep DUT power on for an additional 10 minutes to allow for heat build up and verify proper operation. Step to next highest temperature (with DUT power off) and again verify proper start up and operation. Keep DUT power on for an additional 10 minutes and verify proper operation. Repeat stepping to determine UOL-T (V-nom).
NOTE— Keeping power off until temperature stabilized is important for achieving proper DUT internal temperatures and verifying start up characteristics. Step size = 5 °C from DUT specified upper operating limit. Limit upper temperature to 15 °C above specified DUT upper operating temperature. If plastics limit UOL-T, consider deleting them so that the true limit of the electronics can be determined.

j. Compute T-hi = UOL-T (V-nom) – 5 °C. The value of T-hi should result in full module operation but not necessarily meet all specs.

k. Repeat Ramp and PAR testing at T-hi. Verify results are similar to that found in steps a to c.

LOL-V (T-hi), (i.e., LOL – Voltage at T-hi)
UOL-V (T-hi), (i.e., UOL – Voltage at T-hi). Note if DUT still operational at 20 V.

l. Repeat step k (at T-hi only) on second DUT and verify similar results.
m. For convenience enter results in Table 1.

TABLE 1—DESIGN MARGIN, CHARACTERIZATION TEST RESULTS

Parameter	DUT Mode	DUT Power	Value, DUT 1	Value, DUT 2	Comments
T-ambient :					
LOL-V (T-amb)					
UOL-V (T-amb)					
T-low :					
LOL-T (V-nom),					
T-lo = LOL-T (V-nom) +5 °C					
LOL-V (T-lo)					
UOL-V (T-lo)					
T-high :					
UOL-T (V-nom)					
T-hi = UOL-T (V-nom) – 5 °C					
LOL-V (T-hi)					
UOL-V (T-hi)					

6.4.2 VOLTAGE INTERRUPTIONS, TRANSIENTS—This section gives details for generating electrical noise either as a separate test or as part on another (e.g., 6.4.1). It addresses the following:

a. Events due to ignition switch or relay bounce.
b. Events due to intermittent connections – combination of contact fretting (corrosion) and vibration (e.g., hitting pothole) can cause intermittent connection (contributor to Trouble Not Indicated – TNI's).
c. Transients and DC noise voltage on the ground and power circuits.

See Figures 3 and 4 for examples of waveforms

Special Equipment:

a. DUT Termination Fixture
b. Electrical Stress Simulator - PAR Tester

Evaluation Method:

a. Refer to Table 2 and Figure 2 for test parameters and waveforms.
b. Connect PAR Tester to power inputs of DUT, one at a time. Activate PAR Tester in modes per Table 2. Verify DUT response per Table 2 Acceptance Criteria.

NOTE— Ensure that Power Supply and DUT active terminations (e.g., signal generators) are not affected by noise generator.

TABLE 2—VOLTAGE INTERRUPTIONS, TRANSIENTS

Test	Desc[1][2][3]	Relay Fig 1	Volt Range	Time Range	Accept Criteria
1	***Power Cycle (PC)***	1	Varies	10 min on, 10 min off	
2A	***Power interrupt during start up***: Uses series chattering relay to generate short burst of power interruptions. Mainly verifies DUT initialization response to power-up (relay or switch bounce).	1, 2, 3			
	Combinations of volt, time duration		Normal 10-16 V	10, 30, 50, 100 ms	I
	Combinations of volt, time duration		Extend 8-20 V	10, 30, 50 100 ms	I, II[4]
2B	***Power interrupt after start up***: Uses series chattering relay to generate series of power interruptions. Verifies DUT response to intermittent power (combination of contact fretting (corrosion) and vibration (e.g. hitting pothole) can cause intermittent connection (contributor to Trouble Not Indicated – TNI's).	1, 2, 3			
2C	***Power interrupt after start up + transients***: Uses series chattering relay and A/C clutch coil in parallel with DUT to generate series of power interruptions and transients.	1, 2, 3, 6			
	Combinations of volt, time duration		Normal 10-16 V	10, 30, 50 ms	II min
	Combinations of volt, time duration		Extend 8-20 V	10, 30, 50 ms	II min
	Combinations of volt, time duration		Normal 10-16 V	100, 300, 500 ms	II min
	Combinations of volt, time duration		Extend 8-20 V	100, 300, 500 ms	II min
3A[5]	***Transients - Chattering Relay***: Chattering relay in parallel with DUT develops voltage drops (DC, transient) across impedance (R1, R2).	1, 4, 5			
3B[5]	***Transients - Induct, Hi Current***: A/C clutch coil and switch in parallel with DUT develops voltage drops (DC, transient) across common impedance (R1, R2).	1, 6			
	Combinations of volt, time duration		Normal 10-16 V	1 s	I
	Combinations of volt, time duration		Extend 8-20 V	1 s	I, II[4]

1. Default values given - other values can be used.
2. Two modes of operation: 1 = Continuous, keeps executing specific test until manually stopped, pause between each combination of parameters to check DUT response. 2 = Cyclic, combines specific tests with power cycle.
3. Power on voltages dependent on DUT and analysis (min defaults = V-nominal, V-high, V-low). Resolution = 0.5 V
4. Response depends on voltages and time durations of stress. Some typical responses shown. For possible DUT responses, see 6.3.
5. This mode (3 A, B) also verifies that a DUT is compatible with noise voltage on the ground and power circuits. Based on analysis, the test should be run in modes where the DUT response could be sensitive to ground and power offsets. Include effects of DUT input offsets – connect switch inputs to ground (or power) on power supply side of PAR Tester so that there is noise between the DUT and the switch.

6.4.3 POWER DIP—This method verifies that a DUT is compatible with power dips most commonly experienced during engine starting. It is also used to evaluate voltage regulator input step response.

Special Equipment:

a. DUT Termination Fixture
b. Electrical Stress Simulator - PAR Tester

Evaluation Method:

a. Activate tester in power dip mode per Table 3. Reference Figure 2 for waveforms.
b. If the DUT contains a new voltage regulator, this test can be used to evaluate regulator stability when exposed to step inputs. Monitor regulator output and look for overshoot, undershoot, oscillations.
c. Monitor DUT after each test point. Default dwell = 10 s or enough to determine DUT response.
d. For DUT's with large power input capacitors and without a reverse protection diode, it may be necessary to use the DC Power Amp output that has a series diode and shunt resistance. This simulates other loads that may be on same power feed to DUT in the vehicle.

TABLE 3—POWER DIP PARAMETERS

Test	Desc	V-hi (V10)	V-lo (V11)	Duration	Separation	Accept Criteria
1A	Single short	13	Hi = 10 Lo=8, 6, 3, 1	0.3, 0.5, 1 ms		Hi = I Lo = I
1B	Single long	13	Hi = 10 Lo=8, 6, 3, 1	10, 100 ms, 1 s		Hi = I Lo = II
2A	Multiple short	13	Hi = 10 Lo=8, 6, 3, 1	0.3, 0.5, 1 ms	1, 5, 10, 100 ms	Hi = I Lo = I
2B	Multiple long	13	Hi = 10 Lo=8, 6, 3, 1	10, 100 ms, 1 s	1, 5, 10, 100 ms	Hi = I Lo = II
2C	Multiple combo	13	Hi = 10 Lo=8, 6, 3, 1	0.3, 0.5, 1 ms, 10, 100 ms, 1 s	1, 5, 10, 100 ms	Hi = I Lo = II

NOTE— Values shown are examples only

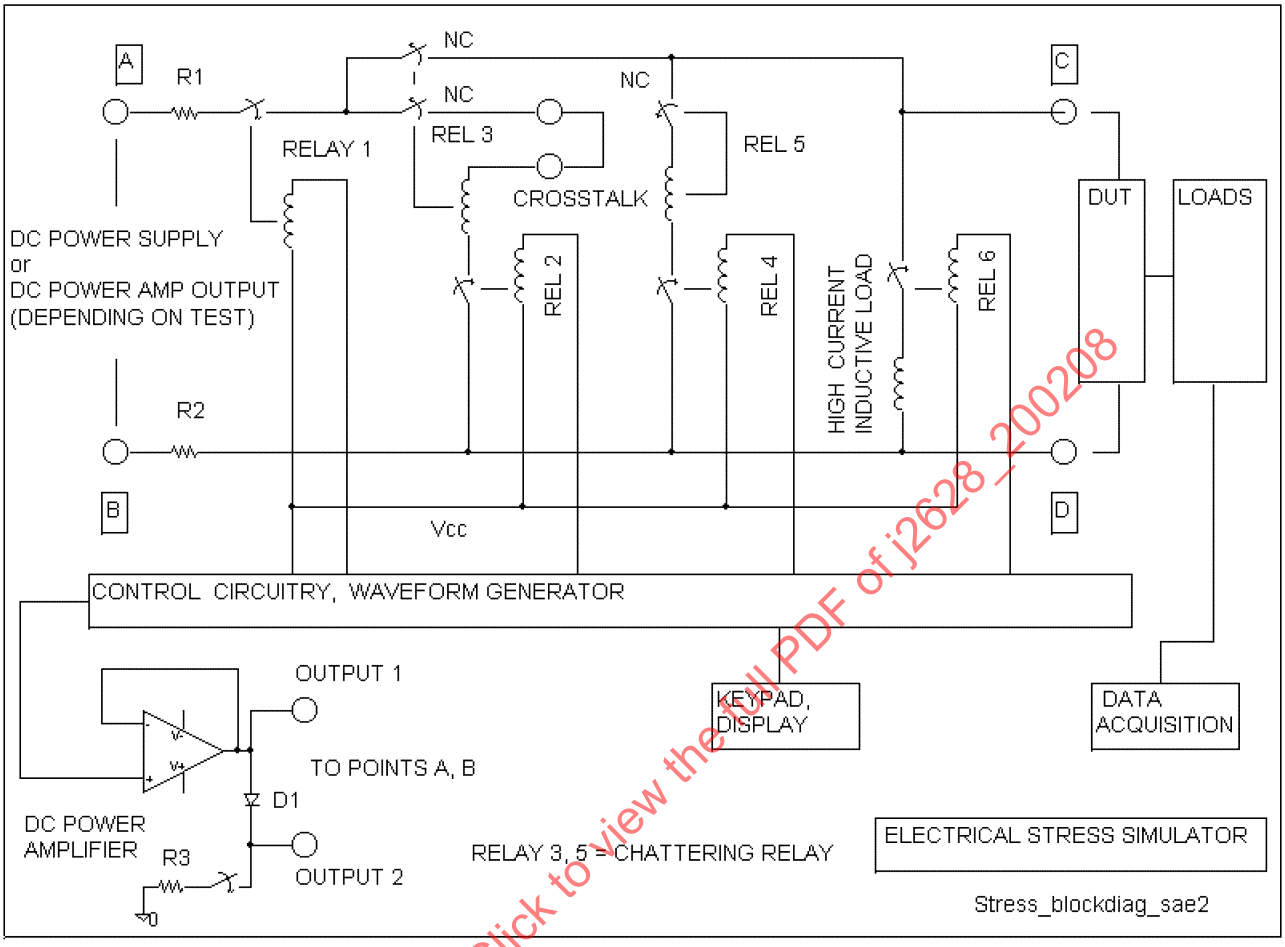

FIGURE 1—ELECTRICAL STRESS SIMULATOR

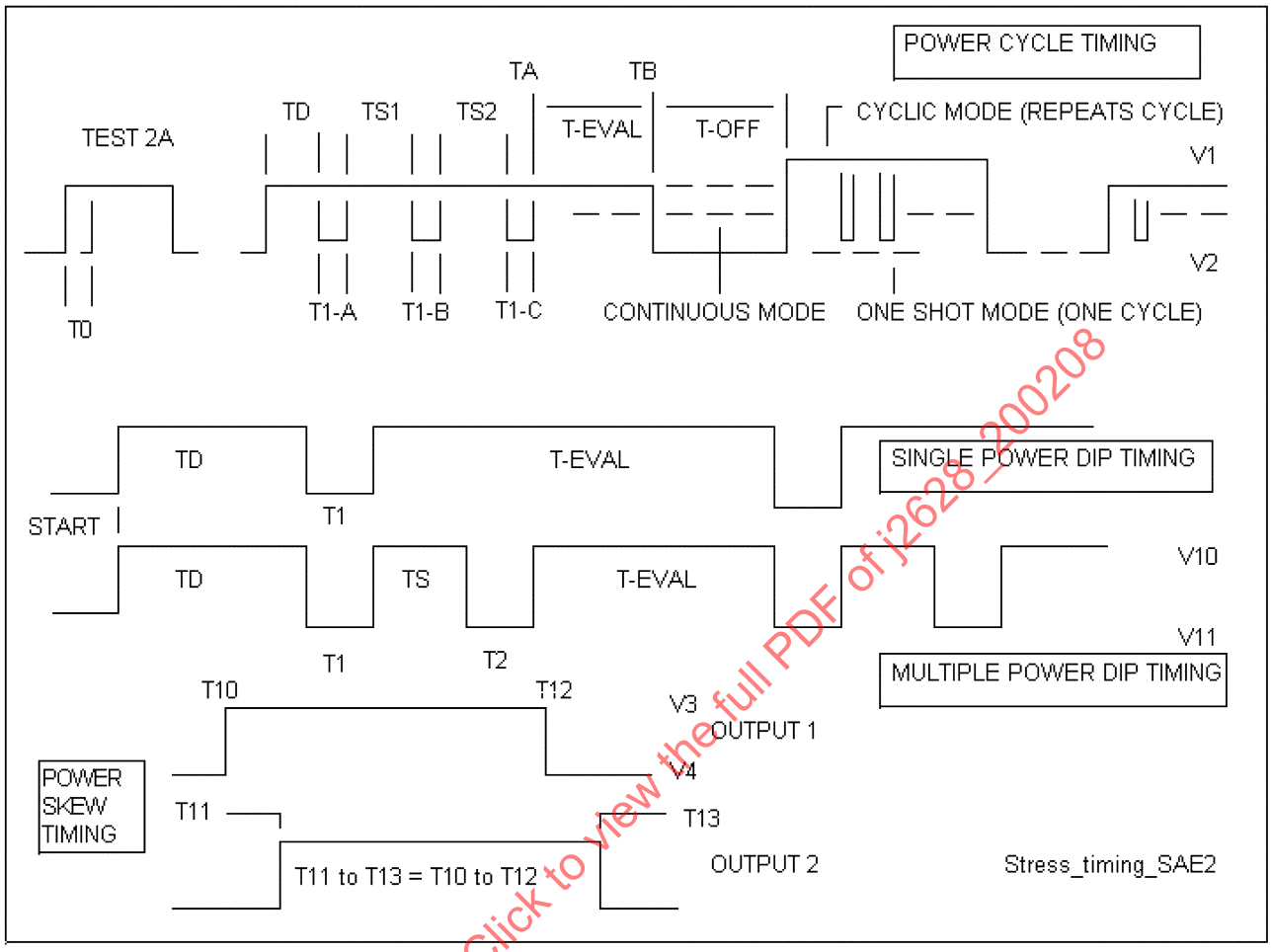

FIGURE 2—TIMING DIAGRAM